Please amend Claim 16 as follows:

16. (Twice amended) A method for fabricating a semiconductor device with a trenched gate comprising:

forming an oxide layer on the surface of a semiconductor substrate;

forming a nitride layer on said oxide layer;

etching a trench having substantially upright vertical sidewalls and a bottom surface in said semiconductor substrate;

forming a trench-to-gate insulating layer inside the trench, wherein the trench-to-gate insulating layer comprises a trench gate dielectric spacer formed on the upright vertical sidewalls inside the trench and a trench gate tunneling dielectric formed on the bottom surface inside the trench;

forming a trenched gate electrode on the trench-to-gate insulating layer inside the trench;

forming a source region and a drain region in the semiconductor substrate such that the source and drain regions partially extend laterally underneath the bottom of the trench;

forming an inter-gate dielectric layer on a top surface of the trenched gate electrode; and

forming a control gate electrode on a top surface of the inter-gate dielectric layer.

Please amend Claim 19 as follows:

19. (Twice amended) A method for fabricating a semiconductor device with a trenched gate comprising:

etching a trench having substantially upright vertical sidewalls and a bottom surface in a semiconductor substrate;

forming a trench-to-gate insulating layer inside the trench, wherein the trench-to-gate insulating layer comprises a trench gate dielectric spacer formed on the upright vertical sidewalls inside the trench and a trench gate tunneling dielectric formed on the bottom surface inside the trench;

forming a trenched gate electrode on the trench-to-gate insulating layer inside the trench;

forming a source region and a drain region in the semiconductor substrate such that the source and drain regions partially extend laterally underneath the bottom of the trench;

forming an inter-gate dielectric layer on a top surface of the trenched gate electrode;

forming a control gate electrode on a top surface of the inter-gate dielectric layer, and

wherein the step of forming a source region and a drain region comprises a self-limiting diffusion process.

21. (New) The method of Claim 16, wherein said nitride is silicon nitride.

22. (New) The method of Claim 21, wherein said nitride is approximately 1500 angstroms thick.

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23. (New) The method of Claim 16, wherein said oxide layer is approximately 100 angstroms thick.

24. (New) The method of Claim 16, further comprising planarizing said trenched gate electrode using said nitride as a stop for the planarization process.

23 (continued)

25. (New) The method of Claim 24, further comprising removing said nitride layer using a plasma etch.

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26. (New) The method of Claim 16, wherein said trench is between approximately 100 angstroms and 5000 angstroms wide.

27. (New) The method of Claim 16, wherein said trench is between approximately 100 angstroms and 5000 angstroms deep.

28. (New) The method of Claim 19, further comprising:
forming an oxide layer on the surface of said semiconductor substrate; and
forming a nitride layer on said oxide layer.

29. (New) The method of Claim 28, wherein said nitride is silicon nitride.

30. (New) The method of Claim 29, wherein said nitride is approximately 1500 angstroms thick.

31. (New) The method of Claim 28, wherein said oxide layer is approximately 100 angstroms thick.

32. (New) The method of Claim 28, further comprising planarizing said trenched gate electrode using said nitride as a stop for the planarization process.

33. (New) The method of Claim 28, further comprising removing said nitride layer using a plasma etch.

34. (New) The method of Claim 28, wherein said trench is between approximately 100 angstroms and 5000 angstroms wide.

35. (New) The method of Claim 28, wherein said trench is between approximately 100 angstroms and 5000 angstroms deep.